INTERRUPT DISABLING APPARATUS, SYSTEM, AND METHOD

ABSTRACT OF THE DISCLOSURE

An interrupt processing apparatus, system, and article including a machine-accessible medium, along with a method of processing interrupts, optimize interrupt-handling by combining the activities of acknowledging and disabling the interrupt. In one embodiment, the apparatus may include an interrupt cause register coupled to an interrupt disabling register and an interrupt mask register. The system may include a processor coupled to an interrupt cause register using a bus, along with an interrupt disabling register coupled to an interrupt mask register and the interrupt disabling register. The method may include reading an interrupt cause register in response to receiving an interrupt, and transferring a mask value stored in an interrupt disabling register directly to an interrupt mask register so as to disable receiving further interrupts from the interrupt source.